Code No: RT22022 **R13** SET - 1

**II B. Tech II Semester Supplementary Examinations, Dec - 2015**
**SWITCHING THEORY AND LOGIC DESIGN**
(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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**PART-A**

1. a) Convert the given Gray code number to equivalent binary 1001001011110010.
   b) Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal.
   c) Implement full adder with 4 to 1 multiplexer.
   d) Implement the Boolean functions with a PLA $F(A,B,C)= \sum(0,1,2,4)$
   e) Explain the differences between asynchronous and synchronous counters.
   f) Draw the diagram of JK flip flop and its truth table. (3M+3M+4M+4M+4M+4M)

**PART-B**

2. a) Prove the following Boolean theorems
   (i) AB+A'C = (A+C)(A'+B) (ii) AB+A'C+BC = AB+A'C
   b) Simplify the following Boolean expressions
   (i) ABC+AB'+ABC' (ii) ACD+A'BCD. (8M+8M)

3. a) Minimize the following expressions using K-map and realize using NAND Gates.
   $f = \sum m (1,3,5,8,9,11,15) + d (2,13)$
   b) Minimize the following expression using K-map and realize using NOR Gates.
   $f = \prod M (1,2,3,8,9,10,11,15) + d (7,1,5)$ (8M+8M)

4. a) Design a combinational circuit whose input is a four bit number and whose output is the 2's complement of the input number.
   b) Implement 64 x 1 multiplexer with four 16 x 1 and one 4 x 1 multiplexer. (8M+8M)

5. a) Explain the operation R-S master slave flip flop. Explain its truth table
   b) Explain about the realization of SR flip-flop, JK flip-flop using D flip-flop. (8M+8M)

6. a) Draw and explain 4-bit universal shift register.
   b) Design a MOD-6 ripple counter. (8M+8M)

7. a) Explain in detail about sequential programmable devices.
   b) Explain in detail about ROM. (8M+8M)
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